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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,928	10/28/2003	Isao Okada	Q78036	4142

23373 7590 02/05/2007

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EXAMINER	
BIBBINS, LATANYA	
ART UNIT	**PAPER NUMBER**
2627	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/693,928	OKADA ET AL.	
	Examiner	Art Unit	
	LaTanya Bibbins	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima (US PGPub 2002/0051415 A1) and further in view of Applicants Admitted Prior Art (hereafter AAPA). It is noted that citations to AAPA refer to the Background of the Invention of Applicant's Specification.

Regarding claim 1, Iijima discloses a recording pulse generator comprising: a first delay line having plural circuit elements cascaded in multiple stages, wherein the first delay line outputs plural output clocks each having different phase differences with a clock inputted to the first stage of the first delay line, according to the number of stages of the plural circuit elements thereof (see Figure 1 element 11 and the discussion in paragraph [0033]). Iijima also discloses a selector that is used to select an arbitrary clock from the plural clocks generated (Figure 1 element 12 and further paragraph [0034]) and a recording pulse generator that generates a recording pulse on the basis of a clock selected from the selector (Figure 1 element 18 and further in paragraph [0041]).

Iijima fails to teach a level shift stage that generates the plural fine clocks to be selected by the selector. AAPA, however, discloses the use of a level shift stage in the recording waveform generator (see Figure 13 element 22).

One of ordinary skill in the art at the time the invention was made would have been motivated to combine the teachings of Iijima with AAPA because it would have been well known in the art at the time of the invention as shown in AAPA.

The combination of Iijima and AAPA discloses the claimed invention except for that the level shift stage is used after the selector. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the level shift stage prior to the selector, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

Regarding claim 4, Iijima and AAPA teach a recording pulse generator as claimed in claim 1, wherein the selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks (see the discussion of the selector in Iijima paragraphs [0035]-[0039]). A selector is simply a switch that connects multiple lines to a single line and as such is equivalent to a multiplexer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made combine the teachings of Iijima and AAPA. One of ordinary skill in the art at the time the invention was made would have been motivated to incorporate the section taught by Iijima into the recording pulse generator of AAPA optimize the phase of the delay clock even when data is being recorded thus enabling the recording

waveform to be accurately generated even when the data is continuously recorded for a long time (see Iijima paragraph [0015]).

3. Claims 2, 3, and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima (US PGPub 2002/0051415 A1) and AAPA as applied to claim 1 above, and further in view of Hayashi et al. (US Patent Number 6,493,305 B1).

Regarding claim 2, Iijima and AAPA teach a recording pulse generator as claimed in claim 1, further comprising a PLL oscillator that possesses an oscillator with plural circuit elements cascaded in multiple stages (see the PLL oscillator of AAPA in Figure 13, specifically VCO2 and cascaded element 2a) and controls a voltage of a power supply line for the first delay line and the oscillator of the PLL oscillators according to the phase comparison result (see the signal Vs which is the output of element 7 in Figure 13).

Iijima and AAPA fail to teach that the PLL oscillator compares the phase of a signal generated by the oscillator with the phase of the clock inputted to the first stage of the first delay line. Hayashi, however, teaches that the PLL oscillator includes a phase comparator that compares the phase of the frequency of the oscillation output signal and the phase of the reference clock (see Hayashi column 9 lines 46-52).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Iijima and AAPA with that of Hayashi. One of ordinary skill in the art at the time the invention was made would have

been motivated to combine the teachings in order to obtain a delay circuit suitable for obtaining a highly accurate and substantially uniform delay line (see Hayashi column 9 lines 31-36).

Regarding claims 3 and 6, Iijima and AAPA fail to teach a recording pulse generator where the clock inputted to the first stage of the first delay line is an EFM clock that varies according to a recording speed. Hayashi however, teaches a recording pulse generator wherein the clock inputted to the first stage of the first delay line is an EFM clock that varies according to a recording speed (see Figures 1 and 3 and the teachings in column 5 lines 24-28 and column1 lines 40-42).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the use of the EFM clock input taught by Hayashi into the recording pulse generator of Iijima and AAPA because EFM reduces errors by minimizing the number of zero-to-one and one-to-zero transitions and small pits and lands are avoided. Disks can be played or written at different speeds; therefore the EFM data needs to be written to the disk at different speeds. As the speed increases, the period of the EFM signal decreases. Therefore the invention as a whole would have been prima facie obvious to one of ordinary skill in the art at the time the invention was made, absent unexpected results to the contrary.

Regarding claims 7-9, Iijima, AAPA, and Hayashi teach a recording pulse generator wherein the selector is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks (see the discussion of the selector in Iijima

paragraphs [0035]-[0039]). A selector is simply a switch that connects multiple lines to a single line and as such is equivalent to a multiplexer.

4. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima (US PGPub 2002/0051415 A1) and AAPA as applied to claim 1 above, and further in view of Kobayashi et al. (US Patent Number 5,818,805).

Regarding claims 5 and 12, Iijima and AAPA fail to teach a recording pulse generator provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer. Kobayashi, however, teaches a recording pulse generator wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer (see the recording signal generating apparatus which uses a T-type flip-flop triggered by the output of a data selector Figure 16 element 18 and column 12 lines 50 and 51; the data selector provides one of eight delayed clock outputs to the T-type flip-flop see Figure 16 element 10 and column 12 lines 28-36).

One of ordinary skill in the art, at the time the invention was made, would have been motivated to combine the teachings of Iijima and AAPA with Kobayashi and would have had a reasonable expectation in producing the claimed invention because Iijima, AAPA, and Kobayashi teach analogous art. Specifically, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a flip-flop to implement the function of the recording waveform generation circuit described by Iijima. It would have been advantageous to use an integrated circuit, such as a flip-flop, versus

combining AND and NAND gates to perform the desired function of the recording waveform generator. Therefore the invention as a whole would have been prima facie obvious to one of ordinary skill in the art at the time the invention was made, absent unexpected results to the contrary.

5. Claims 10, 11, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iijima (US PGPub 2002/0051415 A1), AAPA, and Hayashi et al. (US Patent Number 6,493,305 B1) and further in view of Kobayashi et al. (US Patent Number 5,818,805).

Regarding claims 10, 11, and 13-16, Iijima, AAPA, and Hayashi fail to teach a recording pulse generator provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer. Kobayashi, however, teaches a recording pulse generator wherein the recording pulse generator is provided with a flip-flop circuit that operates based on a delayed clock selected by a multiplexer (see the recording signal generating apparatus which uses a T-type flip-flop triggered by the output of a data selector Figure 16 element 18 and column 12 lines 50 and 51; the data selector provides one of eight delayed clock outputs to the T-type flip-flop see Figure 16 element 10 and column 12 lines 28-36).

One of ordinary skill in the art, at the time the invention was made, would have been motivated to combine the teachings of Iijima, AAPA and Hayashi with Kobayashi and would have had a reasonable expectation in producing the claimed invention because Iijima, AAPA, Hayashi and Kobayashi teach analogous art. Specifically, it

would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a flip-flop to implement the function of the recording waveform generation circuit described by Iijima. It would have been advantageous to use an integrated circuit, such as a flip-flop, versus combining AND and NAND gates to perform the desired function of the recording waveform generator. Therefore the invention as a whole would have been prima facie obvious to one of ordinary skill in the art at the time the invention was made, absent unexpected results to the contrary.

Response to Arguments

1. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaTanya Bibbins whose telephone number is (571) 270-1125. The examiner can normally be reached on Monday through Friday 7:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on 571 272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LaTanya Bibbins

THANG V. TRAN
PRIMARY EXAMINER